

CLAIMS

What is claimed is:

- 1 1. A method for determining the logic state of a memory cell in a
2 magnetic tunnel junction (MTJ) memory device, comprising the steps of:
3 applying a first bias voltage to the cell;
4 measuring a current flowing through the cell at the first bias voltage;
5 applying a second bias voltage to the cell, the second bias voltage being
6 different from the first bias voltage;
7 measuring a current flowing through the cell at the second bias voltage;
8 determining a ratio of the current flowing through the cell at the first bias
9 voltage with the current flowing through the cell at the second bias voltage; and
10 comparing the determined ratio to a predetermined value.
- 1 2. The method of claim 1, wherein the second bias voltage is less than the
2 first bias voltage.
- 1 3. The method of claim 1, wherein the second bias voltage is greater than
2 the first bias voltage.
- 1 4. The method of claim 1, wherein the second bias voltage is on the order
2 of 1/3 of the first bias voltage.

1 5. The method of claim 1, wherein the predetermined value is determined
2 by the steps of:

3 applying a first bias voltage to a reference MTJ memory cell, the state of said
4 reference device being known;

5 measuring a current flowing through the reference cell at the first bias voltage;

6 applying a second bias voltage to the reference cell, the second bias voltage
7 being different from the first bias voltage;

8 measuring a current flowing through the reference cell at the second bias
9 voltage; and

10 determining a ratio of the current flowing through the reference cell at the first
11 bias voltage with the current flowing through the reference cell at the second bias
12 voltage.

1 6. The method of claim 1, wherein the MTJ device is a magnetic random
2 access memory (MRAM).

1 7. The method of claim 6, wherein the MRAM is an MRAM array.

1 8. A system for determining the logic state of a memory cell in a magnetic
2 tunnel junction (MTJ) memory device, comprising:

3 a biasing circuit configured to supply at least two different biasing voltages to
4 the cell;

5 a sensing circuit configured to measure the current flowing through the cell at
6 each of the at least two different biasing voltages; and

7 a processing element configured to determine a ratio of the current flowing
8 through the cell at a first one of the at least two different biasing voltages to the
9 current flowing through the cell at a second one of the at least two different biasing
10 voltages and to compare the ratio to a predetermined value.

1 9. The system of claim 8, wherein the biasing circuit, the sensing circuit,
2 the processing element and the MTJ device are fabricated as an application specific
3 integrated circuit (ASIC).

1 10. The system of claim 8, wherein the biasing circuit is a voltage supply.

1 11. The system of claim 8, wherein the sensing circuit is an ammeter.

1 12. The system of claim 8, further comprising a reference MTJ memory
2 cell having a known state.

1 13. The system of claim 8, wherein the MTJ device is a magnetic random
2 access memory (MRAM).

1 14. The system of claim 10, wherein the MRAM is an MRAM array.

1 15. A computer readable medium for facilitating the determination of the
2 logic state of a memory cell in a magnetic tunnel junction (MTJ) memory device,
3 comprising:

4 logic configured to apply a first bias voltage to the cell and a second bias
5 voltage to the cell, the second voltage being different from the first bias voltage;

6 logic configured to measure a first current flowing through the cell at the first
7 bias voltage and a second current flowing through the cell at the second bias voltage;

8 logic configured to determine a ratio of the first current to the second current
9 and compare the ratio to a predetermined value.

1 16. The computer readable medium of claim 15, wherein the second bias
2 voltage is less than the first bias voltage.

1 17. The computer readable medium of claim 15, wherein the second bias
2 voltage is more than the first bias voltage.

1 18. The computer readable medium of claim 15, wherein the second bias
2 voltage is on the order of 1/3 of the first bias voltage.

1 19. The computer readable medium of claim 15, wherein the
2 predetermined value is determined by:

3 logic configured to apply a first bias voltage and a second bias voltage to a
4 reference MTJ memory cell having a known logic state;

5 logic configured to measure a first current flowing through the reference cell at
6 the first bias voltage and a second current flowing through the reference cell at the
7 second bias voltage; and

8 logic configured to determine a ratio of the current flowing through the
9 reference device at the first bias voltage with the current flowing through the reference
10 device at the second bias voltage.

1 20. The computer readable medium of claim 15, wherein the MTJ device is
2 a magnetic random access memory (MRAM).